Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NECD547	VLSI Architecture for Image and Video Processing	3	0	0	3

Course Objectives

The objective of this course is to impart knowledge on

- To analyze the Image and Video processing algorithms.
- To explore various processing techniques of Image and Video signals.
- To design different architectures of Image and Video signals.

Learning Outcomes

Upon successful completion of this course, the students will:

- Apply various architectures to realize Image processing algorithms.
- Analyze the pipeline architectures for image processing
- Implementation of Low level 2D and 3D and Intermediate level algorithms.
- Evaluate the performances of video processing algorithms.
- Implement various architectures for video Processing.

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Introduction, Image Processing Tasks, Low level Image Processing Operations, Description of some intermediate level operations, Requirements for Image processor architecture.	07	Exposure towards image processing algorithms
2	DSPs and microprocessors, embodiment, alternatives, memory architecture, addressing, pipelining-on-chip, debugging, power consumption and management, clocking, application support, choosing processor architecturetrends. Standard digital signal processors, Application specific ICs for DSP.	08	To get the exposure on processor where the image processing is to be deployed
3	Standard DSP and Ideal DSP architectures, Multiprocessors and multicomputer, message based architectures, Systolic and Wave front arrays, Shared memory architectures. SHARC and Blackfin processors, Architecture, overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations.	09	To get the exposure on architecture of processor where the image processing techniques are to be deployed
4	Mapping of DSP algorithms onto hardware, Uniprocessor architectures, Isomorphic mapping of SFGs, Implementation based on complex Pes, vector-multiplier based implementations, numerically equivalent implementation, implementation of WDFs, Shared memory architecture with Bit, serial PEs, building the large DSP systems, Single Instruction Computer (SIC).	09	To design and synthesis the architecture of DSP processor where image processing will be deployed.
5	Bit-Serial Arithmetic, Bit-Serial Two-Port Adaptor 8 S/P Multipliers with Fixed Coefficients Minimum Number of Basic Operations, Bit-Serial Squares, Serial/Serial Multipliers, Digit-Serial Arithmetic, Cordic Algorithm, Distributed Arithmetic, The Basic Shift-Accumulator, Reducing The Memory Size, Complex Multipliers, Improved ShiftAccumulator, FFT Processor, Twiddle Factor PE, Control PEs, Address PEs, Base Index Generator, Ram Address PEs .	09	To get the exposure on the processing elements available those are suitable for image processing
	Total	**42**	

Textbook:

1. Lars Wanhammer, "DSP Integrated Circuits", Elsevier India Pvt. Ltd, New York, 2012.
2. Phil Lapsley, Jeff Bier, AmitSholam and Edward A.Lee, "DSP Processor Fundamentals-Architectures, and Features", Wiley India, reprint 2011.

Reference Books:

1. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2013.
2. Steven W. Smith, "The Scientist and Engineer's Guide to Digital Signal Processing", 1998
3. P.P.Vaidyanathan, Multirate Systems & Filter Banks, Prentice Hall, Englewood cliffs, NJ, 1993